Good morning,
You are invited to attend our weekly ECE Graduate Seminar.

Old Dominion University
College of Engineering and Technology
Department of Electrical and Computer Engineering

All lectures to be held at 3:00pm on Fridays online at
https://vs.prod.odu.edu/kvs/interface_webex/?cid=202010_ECE7831VS_91606.
For more information, contact Dr. Chung Hao Chen at (757) 683-3475 or email cxchen@odu.edu.

Friday, November 6th Seminar Topic:
CHARACTERIZING SIDE-CHANNEL RESILIENCE OF LOGICAL REDUNDANCY FOR SECURE HARDWARE by Dr. Waleed Al-Assadi, PhD, Associate Professor in the Department of Electrical & Computer Engineering at Old Dominion University

Abstract:

In this work, an algorithm is developed to detect and localize a type of Trojan hardware like logic redundancy. Logic redundancy, while it does not affect functionality of the circuits, it does however change the electrical strength of netlist nodes causing either excessive delay or excessive power dissipation or both. We use the power-delay product (PDP) model as a parameter to detect any unintended changes in the inner modes of the circuit and observe the changes in PDP at primary output nodes of the circuit. Xilinx Vivado design tools was utilized on ISCAS 85 circuits. The algorithm is written in python language.

Bio:

Waleed Al-Assadi received his Ph.D. in Electrical Engineering with emphasis on Computer Engineering. He has over 7 years of industrial experience in microprocessors design at AMD and IBM Microelectronics. He has over 15 years of academic work at Missouri S&T and the University of South Alabama. He is a Sr. member of IEEE, HKN, Tau-Beta- Pi, and Sigma-Xi. He holds 3 USA patents.