Syllabus

ECE 777/ 877:
Semiconductor Process Technology
Fall 2012

1. General:
Meeting Time: Wednesday: 7:10 pm – 9:50 pm
Location: KAUF 224
Instructor: Dr. Helmut Baumgart,
Office hours: Wednesday: 3:30pm – 7:00pm in KH 231-E and by appointment
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2. Course Description:

The course provides an overview of the foundations of microelectronic fabrication technology, which entered into the Nanotechnology Era around the year 2000 consistent with Moore’s Law. The success of microelectronic fabrication technology relies on continuous improvement of integrated circuit performance. This continuous need for device scaling is summarized in Moore’s Law which postulates that the level of chip complexity that can be manufactured for minimal cost is an exponential function that doubles in a period of time. The rate of doubling was originally every year and has since then slowed down to a doubling every two years due to rising chip complexity. This improvement is achieved by reducing (scaling) the dimensions of key components of these electronic systems – the metal oxide semiconductor field effect transistor (MOSFET).

During the past 40 years the microelectronics industry has driven transistor feature size scaling from 10 um well into the 40nm range. Simultaneously, the cost per transistor has decreased by seven orders of magnitude during that timeframe. Scaling consists primarily of reducing feature size and shrinking solid state devices to permit more devices to be placed in a given area of silicon on a wafer. Driven by tremendous advances in lithography and processing technology the 65nm logic technology node is currently entering high volume production at leading semiconductor electronics companies. The inevitable result of continuously shrinking solid state device geometries over decades has been the transformation of traditional microelectronics to nanoelectronics, as it is referred today. In broad terms Nanotechnology is defined as research and technology development at the atomic, molecular or macromolecular level in the length scale of 1-100nm. It is widely expected that these historical scaling trends will continue for at least another 10-20 years, resulting in chips that contain billions of components.

Semiconductor technology is the engine room of the New Economy. Change is endemic. For 45 years, we have had a continuous improvement in IC functional capability with smaller size, increased reliability and lower cost. The market will be around $300B by mid-decade but it has also enabled the growth of the whole computing and electronics segment which is about 10 times larger and that in turn is now driving (though perhaps not enough) almost all other parts of the economy. To make full use of this leverage, a lot of basic features about semiconductor process technology should be understood.
Silicon integrated circuit fabrication technology requires many diverse fields of science and engineering. This course will teach the key fabrication technologies and the scientific foundations that carried microelectronics well into nanotechnology. The topics that are covered include:

3. Course Objectives:

Chapter 1: Introduction/ Invention of the Transistor/ Emergence of Silicon Valley/ Moore’s Law
Chapter 2: Modern CMOS Technology
Chapter 3: Crystal Growth and Wafer Engineering
Chapter 4: Semiconductor Manufacturing, Gettering and Wafer Cleaning
Chapter 5: Lithography and Pattern Transfer
Chapter 6: Thermal Oxidation and the Si/ SiO₂ Interface
  Rapid Thermal Processing
Chapter 7: Dopant Diffusion
Chapter 8: Ion Implantation
Chapter 9: Thin Film Deposition and Epitaxy
  [Atomic Layer Deposition (ALD) of high-k dielectrics]
Chapter 10: Etching
Chapter 11: Back-end Technology
Chapter 12: Statistical Process Control and Process Monitoring in Semiconductor Fabrication

In addition to the regular class room lectures a few educational DVD movies will be shown introducing the operation of a modern semiconductor clean room facility with emphasis on the crucial unit processes and process engineering.

This course is also addressing the technical challenges of progressing deeper into nanotechnology beyond the 45nm node which poses serious technological hurdles. The International Technology Roadmap for Semiconductors (ITRS) has outlined the challenges for front-end processes (FEOL) in terms of materials- limited device scaling.

Beyond the 45nm node the thickness of SiO₂ based gate oxides need to be reduced to < 1nm. At these dielectric thicknesses key dielectric parameters like gate leakage current and oxide breakdown degrade seriously. A potential solution is offered by replacing conventional SiO₂ with high dielectric constant (k) gate stacks. High-k insulators can be grown physically thicker for the same (or thinner) equivalent oxide thickness (EOT) and thus provide a significant gate leakage reduction. The current system of silicon dioxide or oxynitride gate dielectric and polysilicon gate electrode has fundamental materials limitations which require the introduction of new materials. More specifically, the ITRS defines near term challenges as: New gate stack processes and materials.

An inherent consequence of the replacement of SiO₂ and SiOₓNᵧ as the gate dielectrics in future generations of CMOS devices is that a new method for the dielectric deposition will be needed too. Atomic Layer Deposition (ALD) is a leading candidate and ALD is recognized as the key technology for the semiconductor industry to break below the 45nm device node barrier in the quest of continuous miniaturization towards ever smaller Nanotechnology nodes. The chapter on Thin Film Deposition will discuss ALD of high-k dielectrics.

Beyond the 22nm node, where gate lengths will become less than 10nm, we may see the emergence of multigate MOSFETs such as FinFETs or double-gate MOSFETs with better
electrostatic control. With feature sizes of 45nm and 32nm under development, Si CMOS technologies are now leading the field of nanotechnology. Silicon CMOS will be the dominant form of nanotechnology and will continue to do so for the foreseeable future. But it is equally clear, that in the long term, CMOS transistor scaling for planar technology must inevitably slow down and finally halt when lithography scale reaches atomic dimensions.

In summary, traditional top-down microelectronics have not only become nanoelectronics, but the device dimensions are now comparable to those being explored in the new field of bottom-up nanotechnology and molecular electronics.

4. Required Main Textbook:

Silicon VLSI Technology: Fundamentals, Practice and Modeling by James D. Plummer, Michael D. Deal and Peter B. Griffin (Prentice Hall Electronics and VLSI Series)

5. Additional Reading:

The Science and Engineering of Microelectronic Fabrication by Stephen A. Campbell (Oxford University Press)

Silicon Processing for the VLSI Era (Volume 1-Process Technology, Volume 2-Process Integration and Volume 3-The Submicron MOSFET) by S. Wolf and R. N. Tauber, Lattice Press, Sunset Beach, California


VLSI Technology by S. M. Sze (McGraw Hill)

6. Student Evaluation:

   Term Paper on Moore’s Law: 20%
   Comprehensive Term Paper Project: 20%
   Powerpoint Presentation Comprehensive: 20%
   Final Exam: 40%

7. Grading:

   \[ \geq 95\% = A; \geq 90\% = A-; \geq 85\% = B+; \geq 80\% = B; \geq 75\% = B-; \geq 70\% = C+; \geq 65\% = C; \geq 60\% = C-; \geq 55\% = D; < 50\% = F \]

8. Class attendance: Mandatory
Blackboard:

I shall post all my lecture notes and all my MS Powerpoint Viewgraphs on Blackboard where you’ll also find Notes, the course Syllabus, Assignments & Messages:

9. Academic Integrity and ODU Honor Code:

As engineers you will be responsible for upholding the canons of ethics of the profession. The Honor System at ODU is based upon the integrity of the individual. This system assumes that the student will accept his or her role in the University community with a feeling of self-respect and duty. Th Honor Pledge (attested by signature) requires that each piece of work submitted by a student is to be his/ her own work unless prepared under other conditions specified by the instructor.

10. Disability:
Students with documented learning disabilities should see the instructor during the first week of class to make proper arrangements.