Course description:
This course covers prerequisite topics for non-computer engineering graduate students interested in studying computer engineering. The course includes two major areas of digital system design and microcontroller design. Topics in digital system design include the use of a hardware description language to specify/design algorithmic state machines, controller design, data & control path design, top-down design of digital systems. Topics in microcontroller design include an overview of microcontroller architectures, assembly language programming, programming, I/O interfacing, and interrupt management. Not open to students already with a BS in Computer engineering or have already taken ECE 341 and ECE 346 or the equivalent. (offered fall)

Prerequisites: ECE 241 or equivalent, CS 150 or equivalent
Leveling Prerequisite for: ECE 541, ECE 543, ECE 648

Textbook(s) and/or other required materials:
Others as needed.
(copy of B1 will be placed on reserve in the library)

Course Learning Objectives:
1. Develop proficiency in modeling digital systems with VHDL
2. Design using algorithmic state machine methods
3. Controller design using structured design approaches including one-hot and microcoded controllers
4. Modeling datapath components including registers, counters, ALUs
5. Create datapath to model complex digital systems
6. Control path design
7. Introduction to FPGA design flow
8. Introduction to microcontroller architecture

Topics Covered:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Periods</th>
<th>Text Sections</th>
</tr>
</thead>
<tbody>
<tr>
<td>I. COURSE INTRODUCTION</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A. Course Overview</td>
<td>1</td>
<td>---</td>
</tr>
<tr>
<td>B. Curriculum Overview</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C. Course Format and Policies</td>
<td></td>
<td></td>
</tr>
<tr>
<td>II. EXTENDED REVIEW</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>III. INTRODUCTION TO VHDL</td>
<td>6</td>
<td>B1: 2.1-2.16</td>
</tr>
<tr>
<td>A. Modeling digital systems with VHDL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B. Concurrent signal assignments</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C. Processes, sequential statements, and delay models</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IV. STATE MACHINE &amp; CONTROLLER DESIGN</td>
<td>3</td>
<td>B1: 5.1-5.5,6.9</td>
</tr>
<tr>
<td>A. State machine diagrams</td>
<td></td>
<td>3.2,3.4</td>
</tr>
<tr>
<td>B. one hot finite state machine design</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C. microcoded controller design</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V. SYSTEM MODELING WITH VHDL</td>
<td>3</td>
<td>6.11,6.12</td>
</tr>
<tr>
<td>A. Introduction to FPGA Design flow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B. Modeling levels of abstraction</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## VI. DATAPATH DESIGN
A. Components, registers, counters, etc
B. Fast adders
C. Multipliers
D. Buses and data movement

## VII. SELECTED TOPICS IN VHDL
A. Functions, procedures, and packages
B. Attributes, IEEE STD_LOGIC
C. Named associations and generate
D. File I/O

## VIII. Introduction to microprocessors

## IX. Assembly language programming
A. Assembler and instruction set
B. Programs, stack, subroutines
C. Interrupts and interrupt service routines

## X. Microcontroller architecture
A. Peripherals
B. Bus timing
C. Interfacing

## XI. SUMMARY AND WRAP-UP

---

**Class Schedule:** MWF Three times a week.  
Each class is 50 minutes duration.

**Grading:**
- Homework: 20%
- Mini-Projects (6): 42%
- Final exam: 28%

**Prepared by:** Lee A. Belfore II

**Signature and Date:** ______________________________